PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-075840

(43)Date of publication of application : 14.03.2000

(51)Int.Cl. G09G 3/36
G02F 1/133

(21)Application number : 10-244772

(22)Date of filing : 31.08.1998

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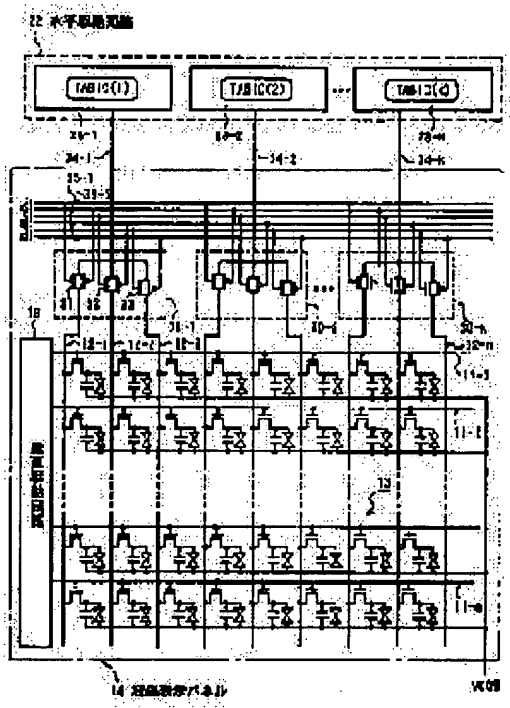
(54) LIQUID CRYSTAL DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a liquid crystal display device, which has a high degree of freedom in arranging a horizontal external IC circuit against the module of a liquid crystal display panel, by constituting the scanning direction of a vertical driving circuit to be reversible vertically.

SOLUTION: The vertical driving circuit 18 is constituted such that, for example, it is provided with a shift register, level shifter and buffer, that its scanning direction (driving direction) is vertically reversible, and that, in other words, it is scannable in either directions. The scanning direction depends on the shift direction (reverse direction) of the shift register, By using this vertical driving circuit 18 scannable in both directions, whether a user arranges an external IC circuit TABIC(1) 28-1 to TABIC (k) 28-k above or below a liquid crystal display panel 14 by preference, he can deal with it by merely changing the scanning direction of the vertical driving circuit 18 in accordance with the arrangement, without externally installing field memory for the purpose of rearranging image data. Consequently, a low cost liquid crystal module is possible.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

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CLAIMS

[Claim(s)]
[Claim 1] The pixel section which comes to form a pixel on a transparence insulating substrate at the intersection of the gate line for a multi-line and the signal line for two or more trains which were wired in the shape of a matrix, The vertical-drive circuit which is prepared on said transparence insulating substrate and carries out selection actuation of the gate line for said multi-line, The liquid crystal display characterized by being prepared on the external circuit substrate of another object, having the level actuation circuit which supplies signal potential one by one to the signal line for said two or more trains, and the scanning direction of said vertical-drive circuit having composition in which vertical reversal is possible with said transparence insulating substrate.
[Claim 2] Said vertical-drive circuit is a liquid crystal display according to claim 1 characterized by the thing by which it was prepared in the one side of the right and left to said pixel section, and for which it consists of an actuation circuit of a single bidirectional scan, and a scanning direction is set up by the control signal from the outside.
[Claim 3] Said vertical-drive circuit is a liquid crystal display according to claim 1 characterized by consisting of an actuation circuit of a bidirectional scan of a couple established in the right-and-left both sides to said pixel section, and both setting up the same scanning direction by the control signal from the outside.
[Claim 4] Said vertical-drive circuit is a liquid crystal display according to claim 1 characterized by consisting of an actuation circuit of a uni-directional scan of a couple established in the right-and-left both sides to said pixel section, and setting each scanning direction as an opposite direction mutually.
[Claim 5] The liquid crystal display according to claim 1 characterized by the thing which carry out pressure up of the electrical potential difference from the outside, and supplies on said transparence insulating substrate in said vertical-drive circuit, and to **********.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the active matrix liquid crystal display which comes to form the level actuation circuit for giving signal potential in order to each pixel per line with a transparence insulating substrate as an external IC circuit on the substrate of another object while forming a vertical-drive circuit by the thin film transistor on a transparence insulating substrate about a liquid crystal display (LCD;Liquid Crystal Display).
[0002]
[Description of the Prior Art] As for the liquid crystal display used for the personal computer, the word processor, etc., the active-matrix mold serves as the main force. This active matrix liquid crystal display is excellent in the field of a speed of response or image quality, and is turning into the optimal liquid crystal display for colorization in recent years.

[0003] Nonlinear components, such as a transistor or diode, are used for each pixel of a liquid crystal display panel in this kind of liquid crystal display. Specifically, it has the structure in which the thin film transistor (TFT;thin film transistor) was formed on the transparence insulating substrate (for example, glass substrate).
[0004] By the way, especially, while forming a vertical-drive circuit by the thin film transistor on a transparence insulating substrate in a large-sized liquid crystal display in recent years, the configuration which formed the level actuation circuit which gives signal potential in order to each pixel per line as an external IC circuit on the external circuit substrate of another object with the transparence insulating substrate is taken.
[0005]
[Problem(s) to be Solved by the Invention] Thus, since the scanning direction (driving direction) of a vertical-drive circuit was immobilization in the one direction conventionally in the liquid crystal display which forms a level actuation circuit in an external IC circuit while forming the vertical-drive circuit by the thin film transistor on the transparence insulating substrate, a degree of freedom will decrease in arrangement (an upper part side side / lower part side of a panel) of the external IC circuit to the module of a liquid crystal display panel, and salability will be missing.
[0006] On the other hand, by taking the configuration supplied to the external IC circuit 102 which is a level actuation circuit, as shown in drawing 10 , after forming a field memory 101 outside and performing a data list substitute by this field memory 101, even if the scanning direction of the vertical-drive circuit 103 is immobilization, it is also enabling the scan of hard flow in the one direction. However, only the part which forms a field memory 101 serves as the cost high in this case.
[0007] This invention has the place which it is made in view of the situation mentioned above, and is made into the object in offering the liquid crystal display with the high degree of freedom of arrangement of a horizontal external IC circuit to the module of a liquid crystal display panel.
[0008]
[Means for Solving the Problem] The pixel section in which it comes to form a pixel at the intersection of the gate line for a multi-line where the liquid crystal display by this invention was wired in the shape of a matrix on the transparence insulating substrate, and the signal line for two or more trains, The vertical-drive circuit which is prepared on a transparence insulating substrate and carries out selection actuation of the gate line for a multi-line, It is prepared on the external circuit substrate of another object, and has the level actuation circuit which supplies signal potential one by one to the signal line for two or more trains, and the scanning direction of a vertical-drive circuit serves as a transparence insulating substrate with the configuration in which vertical reversal is possible.
[0009] In the liquid crystal display of the above-mentioned configuration, even if it does not prepare outside the field memory for performing an image data list substitute even if it is the case where the scanning direction has arranged the horizontal scanning circuit to any of the upper and lower sides to the pixel section by preparing the vertical-drive circuit in which vertical reversal is possible, a response becomes possible only by changing the scanning direction of a vertical-drive circuit according to the arrangement.

[0010]
[Embodiment of the Invention] Hereafter, it explains to a detail, referring to a drawing about the gestalt of operation of this invention.
[0011] Drawing 1 is the outline block diagram showing the active matrix liquid crystal display concerning the 1st operation gestalt of this invention. In drawing 1 , the gate line 11-1 for m lines - 11-m, and the signal line 12-1 for n train - 12-n are wired in the shape of a matrix on a transparence insulating substrate (not shown), for example, a glass substrate, the unit pixel 13 for a m line n train is formed in the intersection, and the liquid crystal display panel 14 is constituted.
[0012] Especially the unit pixel 13 consists of a thin film transistor (pixel transistor) 15, addition capacity 16, and liquid crystal capacity 17 so that clearly from drawing 2 . The gate electrode is connected to the gate line 11-1, 11-2, 11-3, and ...., and, as for the thin film transistor 15, the source electrode is connected to a signal line 12-1, 12-2, 12-3, and .., respectively.
[0013] In this pixel structure, the liquid crystal capacity 17 means the capacity generated between the pixel electrode formed by the thin film transistor 15, and the counterelectrode countered and formed in this. And the potential held at this pixel electrode is written in with the potential of "H" level or "L" level.
[0014] Moreover, in the unit pixel 13, if a thin film transistor 15 will be in an ON state, while the permeability of the light in liquid crystal changes, the addition capacity 16 will be charged. By this charge, it is held until a thin film transistor 15 will be [the light transmittance condition in the liquid crystal by the charge electrical potential difference of the addition capacity 16] in an ON state next, even if a thin film transistor 15 will be in an OFF state. By such method, improvement in image quality in the display image of the liquid crystal display panel 14 is achieved.
[0015] On the same substrate as the liquid crystal display panel 14, the vertical-drive circuit 18 is formed of the thin film transistor. This vertical-drive circuit 18 performs a vertical scanning by giving a scan pulse in order to the gate line 11-1 where one edge each was connected to the outgoing end of each of that line - 11-m, and choosing each pixel 13 per line.
[0016] On the other hand, the level actuation circuit 22 which gives the signal potential according to image data to a signal line 12-1 - 12-n is formed on the circuit board of another object with the substrate of the above-mentioned liquid crystal display panel 14, and is prepared as an external circuit so that it may mention later. In this level actuation circuit 22, when premised on the input of a digital signal, in order to drive liquid crystal, it is necessary to change into an analog signal. The digital image data which enables the display of 512 or more colors with 8 or more gradation is inputted into this level actuation circuit 22.
[0017] Moreover, in order to realize time-sharing actuation which enables a number of the output pin (output terminal) of a driver IC of cutbacks which constitute the level actuation circuit 22 The number corresponding to the number of time sharing for the signal line 12-1 for n train - 12-n (in this example) [when three are divided as one unit (block) corresponding to 3 time sharing] the level actuation circuit 22 k driver ICs corresponding to [so that clearly from drawing 1] the several k divided, for example, TAB(Tape Automated Bonding) IC, (1) 28-1 - TABIC (k) It is constituted by 28-k.
[0018] And these TABIC(s) (1) 28-1 - TABIC (k) 28-k is carried on the external circuit substrate (not shown) of another object with the substrate of the liquid crystal display panel 14, and outputs the signal potential given to two or more signal lines in 1 division block by time series. Corresponding to this, k time division switches 30-1 - 30-k are prepared in the input stage of the signal line 12-1 for n train - 12-n.
[0019] In order to realize 3 time sharing, a time division switch 30-1 consists of three CMOS analog switches (transmission switch) 31, 32, and 33 with which it connects with juxtaposition and a PchMOS transistor and a NchMOS transistor become, and is formed of the thin film transistor on the same substrate as the liquid crystal display panel 14 so that especially clearly from drawing 2 . Also about other time division switches 30-2 - 30-k, it has the completely same composition as a time division switch 30-1.
[0020] And, for example in the time division switch 30-1, each input edge of three analog switches 31, 32, and 33 is connected in common, and the common node is connected to the outgoing end of TABIC 28-1 through the common signal line 34-1. Thereby, it is TABIC (1). The signal potential outputted by time series is given to each input edge of three analog switches 31, 32, and 33 via the common signal line 34-1 from 28-1. Each outgoing end of these analog switches 31, 32, and 33 is connected to one edge each of three signal lines 12-1, 12-2, and 12-3.
[0021] To a time division switch 30-2, it goes via the common signal line 34-2, and is TABIC (2). The signal potential of time series is supplied from 28-2. Similarly, to time division switch 30-k, it goes via common signal-line 34-k, and is TABIC (k). The signal potential of time series is supplied from 28-k. In addition, although the configuration which allotted one common signal line per TABIC was shown by this example since it was easy, two or more common signal lines will be allotted actually.
[0022] Moreover, 2 per analog switch and a total of six control lines 35-1 to 35-6 are wired along the wiring direction

of the gate line 11-1 - 11-m on the same substrate as the liquid crystal display panel 14. And if it is in a time division switch 30-1, for example, two control-input edges of an analog switch 32 are connected to a control line 35-3 and 35-4, and two control-input edges of an analog switch 33 are connected to a control line 35-1 and 35-2 for two control-input edges (namely, each gate of Nch and a PchMOS transistor) of an analog switch 31 a control line 35-5 and 35-6, respectively.

[0023] In addition, although the connection relation to six control lines 35-1 to 35-6 of three analog switches 31-33 of a time division switch 30-1 was explained, it has connection relation with the same completely said of other time division switches 30-2 - the 30-k here.

[0024] The selection pulses S1-S3 for choosing three analog switches 31-33 each of a time division switch 30-1 - 30-k, and XS1-XS3 are given from the outside to six control lines 35-1 to 35-6. Here, the selection pulses XS1-XS3 are reversal pulses of the selection pulses S1-S3. These selection pulses S1-S3, and XS1-XS3 are the signals for carrying out sequential ON of the three analog switches 31-33 each of a time division switch 30-1 - 30-k synchronizing with the signal potential of the time series outputted from each of TABIC 28-1 - 28-k.

[0025] In the liquid crystal display concerning the 1st operation gestalt of the above-mentioned configuration, the vertical-drive circuit 18 has a shift register, a level shifter, and a buffer, and vertical reversal of the scanning direction (driving direction) is attained the composition which can be scanned bidirectionally. The scanning direction is decided by the shift direction (direction of transfer) of a shift register.

[0026] An example of the circuitry of the shift register used for this vertical-drive circuit 18 is shown in drawing 3 . Each transfer stage serves as circuitry which consists of a latching clocked inverter, and the shift register concerning this example indicates the circuitry of transfer [the n+1st step of] stage to be the n-th step to drawing 3 . Here, the circuitry of transfer [the n-th step of] stage shall be taken and explained to an example.

[0027] In drawing 3 between the VDD line 41 and the GND line 42 The PMOS transistors Qp11 and Qp12 and the NMOS transistors Qn11 and Qn12 are connected to a serial. And each gate of the PMOS transistor Qp11 and the NMOS transistor Qn12 is connected in common. The clocked inverter 43 is constituted by impressing Clock CK to the gate of the PMOS transistor Qp12, and impressing Clock XCK (opposite phase of Clock CK) to the gate of the NMOS transistor Qn11, respectively.

[0028] Similarly, between the VDD line 41 and the GND line 42, the PMOS transistors Qp13 and Qp14 and the NMOS transistors Qn13 and Qn14 are connected to a serial, and each gate of the PMOS transistor Qp13 and the NMOS transistor Qn14 is connected in common, and the clocked inverter 44 is constituted by impressing Clock XCK to the gate of the PMOS transistor Qp14, and impressing Clock CK to the gate of the NMOS transistor Qn13, respectively.

[0029] In the configuration mentioned above, a transfer pulse is given to the common gate node of the PMOS transistor Qp11 which is the input edge of a clocked inverter 43, and the NMOS transistor Qn12 through the transfer line 45 from the transfer stage of the preceding paragraph (n-1 step). And the drain common node of the PMOS transistor Qp14 which is the outgoing end of a clocked inverter 44, and the NMOS transistor Qn13 is connected at the drain common node of the PMOS transistor Qp12 which is the outgoing end, and the NMOS transistor Qn11.

[0030] Moreover, CMOS inverter 46 which consists of the PMOS transistor Qp15 and the NMOS transistor Qn15 to which it connected with the serial and the gate was connected in common is formed between the VDD line 41 and the GND line 42. Parallel connection of this CMOS inverter 46 is carried out to hard flow to a clocked inverter 44, and it constitutes the latch circuit.

[0031] That is, the drain common node of the PMOS transistor Qp15 which is the outgoing end, and the NMOS transistor Qn15 is connected to the drain common node of the PMOS transistor Qp14 whose common gate node of the PMOS transistor Qp15 which is the input edge of CMOS inverter 46, and the NMOS transistor Qn15 is the outgoing end of a clocked inverter 44, and the NMOS transistor Qn13 at the common gate node of the PMOS transistor Qp14 which is the input edge of a clocked inverter 44, and the NMOS transistor Qn13, respectively.

[0032] The latch output of a latch circuit which consists of a clocked inverter 44 and CMOS inverter 46 is outputted to the transfer line 48 through CMOS inverter 47 which consists of the PMOS transistor Qp16 and the NMOS transistor Qn16 by which connected with the serial and the gate was connected in common between the VDD line 41 and the GND line 42.

[0033] ...., n-2 steps, n steps, n+2 steps, each input edge of .., and each outgoing end of .., n-1 step, n+1 step, and .. are connected to the transfer line 45, respectively. Moreover, each outgoing end of ...., n-2 steps, n steps, n+2 steps, and .., and .., n-1 step, n+1 step and each input edge of .. are connected to the transfer line 48, respectively.

[0034] CMOS switch 49n is allotted between the input edge of the transfer line 45, for example, transfer [the n-th step of] stage, and the outgoing end of transfer [the n+1st step of] stage, and CMOS switch 50n is allotted between the transfer line 48, for example, n steps of outgoing ends, and n+1 step of input edge. And the control signal (DC bias) for controlling a direction of transfer is given to the CMOS switches 49n and 50n through control lines 51 and 52.

[0035] Next, the circuit actuation for every direction of transfer of the vertical-drive circuit 18 which can be scanned in

both directions of the above-mentioned configuration is explained.
[0036] First, the case of the transfer to down [down / of drawing 1], i.e., the left from the right of drawing 4 R> 4, is explained using drawing 4 . In the transfer to down [this], the DC bias of "H" level and a control line 52 serves as [the DC bias of a control line 51] "L" level. Then, in transfer [the n-th step of] stage, an OFF state and CMOS switch 50n will be [CMOS switch 49n] in an ON state. Moreover, in transfer [the n+1st step of] stage, CMOS switch 49n+1 will be in an ON state, and CMOS switch 50n+1 will be in an OFF state.
[0037] In this condition, the transfer pulse outputted from transfer [the n-1st step of] stage After being inputted into transfer [the n-th step of] stage and passing through this transfer [the n-th step of] stage, it is inputted into transfer [the n+1st step of] stage via CMOS switch 50n. CMOS switch 49n+1 after passing through this transfer [the n+1st step of] stage -- going -- transfer [the n+2nd step of] stage -- ** -- it will be transmitted leftward (the direction of an arrow head in drawing) in order from the right of drawing at the condition to say.
[0038] Next, the case of the transfer to above [above / of drawing 1], i.e., the right from the left of drawing 5 R> 5, is explained using drawing 5 . Besides, in the transfer to a direction, the DC bias of "L" level and a control line 52 serves as [the DC bias of a control line 51] "H" level. Then, in transfer [the n+1st step of] stage, CMOS switch 49n+1 will be in an OFF state, and CMOS switch 50n+1 will be in an ON state. Moreover, in transfer [the n-th step of] stage, an ON state and CMOS switch 50n will be [CMOS switch 49n] in an OFF state.
[0039] In this condition, the transfer pulse outputted from transfer [the n+2nd step of] stage It is inputted into transfer [the n+1st step of] stage via CMOS switch 50n+1. After passing through this transfer [the n+1st step of] stage, it is inputted into transfer [the n-th step of] stage via CMOS switch 49n. CMOS switch 50n-1 after passing through this transfer [the n-th step of] stage -- going -- transfer [the n-1st step of] stage -- ** -- it will be transmitted rightward (the direction of an arrow head in drawing) in order from the left of drawing at the condition to say.
[0040] In the vertical-drive circuit of the above-mentioned configuration, as a control signal which controls a scanning direction, a DC bias will only be given to control lines 51 and 52, and a scanning direction can be controlled easily.
[0041] Thus, by using the vertical-drive circuit which can be scanned bidirectionally as a vertical-drive circuit 18 of drawing 1 TABIC (1) which is an external IC circuit 28-1 - TABIC(k)28-k -- a user -- liking -- responding -- the upper and lower sides of the liquid crystal display panel 14, even if it arranges to any In order for what is necessary just to be to change the scanning direction of the vertical-drive circuit 18 according to the arrangement even if it does not prepare the field memory for performing an image data list substitute outside, it is low cost and a flexible liquid crystal module becomes possible.
[0042] In addition, as shown in drawing 1 , although [this operation gestalt] the vertical-drive circuit 18 in which a bidirectional scan is possible is arranged only to one side (left-hand side) to the pixel section of the liquid crystal display panel 14, you may make it arrange the vertical-drive circuits 18A and 18B of the couple in which both bidirectional scans are possible on both sides of the pixel section of the liquid crystal display panel 14, as shown in drawing 6 .
[0043] Thus, since a scan pulse can be inputted from the both sides of the liquid crystal display panel 14 when the vertical-drive circuits 18A and 18B in which a bidirectional scan is possible have been arranged on both sides of the pixel section of the liquid crystal display panel 14, the difference according to the pixel location in the horizontal direction of the propagation delay of the scan pulse resulting from wiring resistance etc. can be made small. Moreover, the configuration of the liquid crystal display panel 14 can be made into bilateral symmetry.
[0044] Moreover, in this operation gestalt, although one vertical-drive circuit 18 (18A, 18B) considered as the configuration in which a bidirectional scan is possible, as shown in drawing 7 , it is able for a scanning direction to arrange the vertical-drive circuits 18a and 18b of the couple of a uni-directional scan of an opposite direction on both sides of the pixel section of the liquid crystal display panel 14, to double both, respectively, and to consider as the vertical-drive circuit in which a bidirectional scan is possible.
[0045] Also in this case, since the circuit of the same configuration will be arranged at the both sides of the liquid crystal display panel 14, the configuration of the liquid crystal display panel 14 can be made into bilateral symmetry. In addition, what is necessary is to constitute the selection so that supply voltage may be selectively supplied with a switch etc., and just to make it forbid supply of supply voltage in the vertical-drive circuit of those who do not use it with the switch concerned, although it is the translation which uses only either of the vertical-drive circuits 18a and 18b of a couple.
[0046] In addition, although considered as the configuration using the time-sharing actuation by the time division switch 30-1 - 30-k in the liquid crystal display concerning this operation gestalt, it is possible to apply also like the liquid crystal display of a configuration of that it is not limited to this configuration and each output of TABIC 28-1 - 28-k, and the signal line 12-1 of the liquid crystal display panel 14 - 12-n have the response relation of 1 to 1.
[0047] Drawing 8 is the outline block diagram showing the liquid crystal display concerning the 2nd operation gestalt of this invention, among drawing, gives the same sign to drawing 1 and an equivalent part, and is shown. In this

operation gestalt, it has composition which builds in the level shifter 36 which is a booster circuit in the liquid crystal display panel 14, carries out pressure up to the electrical potential difference of the high level which exceeds 5V, for example for the electrical potential difference of the low not more than 5V given from the outside, and supplies the vertical-drive circuit 18.

[0048] By the way, in the component used for a liquid crystal display like a-Si (amorphous silicon) or poly-Si (polish recon), generally, since it is high compared with LSI usual in the threshold voltage Vth, the actuation level as an external interface becomes high. On the other hand, the power source of the surrounding drive system of the liquid crystal display panel 14 is in the inclination of low-battery-izing for the purpose of reduction of power consumption.

[0049] However, positive actuation of the vertical-drive circuit 18 can be realized, maintaining low-battery-ization of the circumference drive system of the liquid crystal display panel 14 by having built in the level shifter 36 in the liquid crystal display panel 14, carrying out pressure up of the electrical potential difference given from the outside, and having made it supply the vertical-drive circuit 18 like the liquid crystal display concerning this operation gestalt.

[0050] An example of the circuitry of the level shifter of a differential mold is shown in drawing 9 . In drawing 9 , the constant current source is constituted between the VDD line 61 and the GND line 62 by connecting the PMOS transistor Qp21 and the NMOS transistor Qn21 to the serial, connecting the gate and the drain of the PMOS transistor Qp21 in common, and connecting the gate of the NMOS transistor Qn21 to the VDD line 61.

[0051] The electrical potential difference from the outside is inputted between an input terminal 63 and 64, an input terminal 63 is a high-level side, and an input terminal 64 is on a low side. Between the VDD line 61 and an input terminal 63, the PMOS transistor Qp22 and the NMOS transistor Qn22 are connected to a serial, and the PMOS transistor Qp23 and the NMOS transistor Qn23 are further connected to the serial. Each gate of the PMOS transistors Qp22 and Qp23 is connected as in common as the gate (drain) of the PMOS transistor Qp21.

[0052] Moreover, between the VDD line 61 and an input terminal 64, the PMOS transistor Qp24 and the NMOS transistor Qn24 are connected to a serial, and the PMOS transistor Qp25 and the NMOS transistor Qn25 are further connected to the serial. And the gate and the drain of the PMOS transistor Qp24 are connected with the gate of the PMOS transistor Qp23 in common, and the gate of the NMOS transistor Qn24 is connected with the gate of the NMOS transistor Qn22, and a drain in common. Moreover, the gate and the drain of the NMOS transistor Qn25 are connected with the gate of the NMOS transistor Qn23 in common.

[0053] In the differential mold level shifter of the above-mentioned configuration, supposing the electrical potential difference of the VDD line 61 is 12V, the level shift of the electrical potential difference an input terminal 63 and whose amplitude inputted among 64 are 3V will be carried out to the electrical potential difference whose amplitude is 12V, and it will be outputted to the vertical-drive circuit 18 from an output terminal 65. In addition, it does not pass over the circuitry mentioned above to an example, but it can use the thing of various circuitry as a level shifter 36.

[0054]

[Effect of the Invention] As explained above, according to this invention, it sets to an active matrix liquid crystal display. By having used the thing of the configuration as a vertical-drive circuit which a scanning direction can vertical reverse an external IC circuit -- a user -- liking -- responding -- the upper and lower sides of a liquid crystal display panel, even if it arranges to any Since it can respond only by changing the scanning direction of a vertical-drive circuit according to the arrangement even if it does not prepare the field memory for performing an image data list substitute outside, it is low cost and a flexible liquid crystal module becomes possible.

[Translation done.]

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Field of the Invention] Especially this invention relates to the active matrix liquid crystal display which comes to form the level actuation circuit for giving signal potential in order to each pixel per line with a transparence insulating substrate as an external IC circuit on the substrate of another object while forming a vertical-drive circuit by the thin film transistor on a transparence insulating substrate about a liquid crystal display (LCD;Liquid Crystal Display).

[Translation done.]

PRIOR ART

[Description of the Prior Art] As for the liquid crystal display used for the personal computer, the word processor, etc., the active-matrix mold serves as the main force. This active matrix liquid crystal display is excellent in the field of a speed of response or image quality, and is turning into the optimal liquid crystal display for colorization in recent years.

[0003] Nonlinear components, such as a transistor or diode, are used for each pixel of a liquid crystal display panel in this kind of liquid crystal display. Specifically, it has the structure in which the thin film transistor (TFT;thin film transistor) was formed on the transparence insulating substrate (for example, glass substrate).
[0004] By the way, especially, while forming a vertical-drive circuit by the thin film transistor on a transparence insulating substrate in a large-sized liquid crystal display in recent years, the configuration which formed the level actuation circuit which gives signal potential in order to each pixel per line as an external IC circuit on the external circuit substrate of another object with the transparence insulating substrate is taken.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to this invention, it sets to an active matrix liquid crystal display. By having used the thing of the configuration as a vertical-drive circuit which a scanning direction can vertical reverse an external IC circuit -- a user -- liking -- responding -- the upper and lower sides of a liquid crystal display panel, even if it arranges to any Since it can respond only by changing the scanning direction of a vertical-drive circuit according to the arrangement even if it does not prepare the field memory for performing an image data list substitute outside, it is low cost and a flexible liquid crystal module becomes possible.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Thus, since the scanning direction (driving direction) of a vertical-drive circuit was immobilization in the one direction conventionally in the liquid crystal display which forms a level actuation circuit in an external IC circuit while forming the vertical-drive circuit by the thin film transistor on the transparence insulating substrate, a degree of freedom will decrease in arrangement (an upper part side side / lower part side of a panel) of the external IC circuit to the module of a liquid crystal display panel, and salability will be missing.
[0006] On the other hand, by taking the configuration supplied to the external IC circuit 102 which is a level actuation circuit, as shown in drawing 10 , after forming a field memory 101 outside and performing a data list substitute by this field memory 101, even if the scanning direction of the vertical-drive circuit 103 is immobilization, it is also enabling the scan of hard flow in the one direction. However, only the part which forms a field memory 101 serves as the cost high in this case.
[0007] This invention has the place which it is made in view of the situation mentioned above, and is made into the object in offering the liquid crystal display with the high degree of freedom of arrangement of a horizontal external IC circuit to the module of a liquid crystal display panel.

[Translation done.]

MEANS

[Means for Solving the Problem] The pixel section in which it comes to form a pixel at the intersection of the gate line for a multi-line where the liquid crystal display by this invention was wired in the shape of a matrix on the transparence insulating substrate, and the signal line for two or more trains, The vertical-drive circuit which is prepared on a transparence insulating substrate and carries out selection actuation of the gate line for a multi-line, It is prepared on the external circuit substrate of another object, and has the level actuation circuit which supplies signal potential one by one to the signal line for two or more trains, and the scanning direction of a vertical-drive circuit serves as a transparence insulating substrate with the configuration in which vertical reversal is possible.
[0009] In the liquid crystal display of the above-mentioned configuration, even if it does not prepare outside the field memory for performing an image data list substitute even if it is the case where the scanning direction has arranged the horizontal scanning circuit to any of the upper and lower sides to the pixel section by preparing the vertical-drive circuit in which vertical reversal is possible, a response becomes possible only by changing the scanning direction of a vertical-drive circuit according to the arrangement.
[0010]
[Embodiment of the Invention] Hereafter, it explains to a detail, referring to a drawing about the gestalt of operation of this invention.
[0011] Drawing 1 is the outline block diagram showing the active matrix liquid crystal display concerning the 1st operation gestalt of this invention. In drawing 1 , the gate line 11-1 for m lines - 11-m, and the signal line 12-1 for n train - 12-n are wired in the shape of a matrix on a transparence insulating substrate (not shown), for example, a glass substrate, the unit pixel 13 for a m line n train is formed in the intersection, and the liquid crystal display panel 14 is constituted.
[0012] Especially the unit pixel 13 consists of a thin film transistor (pixel transistor) 15, addition capacity 16, and liquid crystal capacity 17 so that clearly from drawing 2 . The gate electrode is connected to the gate line 11-1, 11-2, 11-3, and ...., and, as for the thin film transistor 15, the source electrode is connected to a signal line 12-1, 12-2, 12-3, and .., respectively.
[0013] In this pixel structure, the liquid crystal capacity 17 means the capacity generated between the pixel electrode formed by the thin film transistor 15, and the counterelectrode countered and formed in this. And the potential held at this pixel electrode is written in with the potential of "H" level or "L" level.
[0014] Moreover, in the unit pixel 13, if a thin film transistor 15 will be in an ON state, while the permeability of the light in liquid crystal changes, the addition capacity 16 will be charged. By this charge, it is held until a thin film transistor 15 will be [the light transmittance condition in the liquid crystal by the charge electrical potential difference of the addition capacity 16] in an ON state next, even if a thin film transistor 15 will be in an OFF state. By such method, improvement in image quality in the display image of the liquid crystal display panel 14 is achieved.
[0015] On the same substrate as the liquid crystal display panel 14, the vertical-drive circuit 18 is formed of the thin film transistor. This vertical-drive circuit 18 performs a vertical scanning by giving a scan pulse in order to the gate line 11-1 where one edge each was connected to the outgoing end of each of that line - 11-m, and choosing each pixel 13 per line.
[0016] On the other hand, the level actuation circuit 22 which gives the signal potential according to image data to a signal line 12-1 - 12-n is formed on the circuit board of another object with the substrate of the above-mentioned liquid crystal display panel 14, and is prepared as an external circuit so that it may mention later. In this level actuation circuit 22, when premised on the input of a digital signal, in order to drive liquid crystal, it is necessary to change into an analog signal. The digital image data which enables the display of 512 or more colors with 8 or more gradation is inputted into this level actuation circuit 22.
[0017] Moreover, in order to realize time-sharing actuation which enables a number of the output pin (output terminal) of a driver IC of cutbacks which constitute the level actuation circuit 22 The number corresponding to the number of time sharing for the signal line 12-1 for n train - 12-n (in this example) [when three are divided as one unit (block)

corresponding to 3 time sharing] the level actuation circuit 22 k driver ICs corresponding to [so that clearly from drawing 1] the several k divided, for example, TAB(Tape Automated Bonding) IC, (1) 28-1 - TABIC (k) It is constituted by 28-k.

[0018] And these TABIC(s) (1) 28-1 - TABIC (k) 28-k is carried on the external circuit substrate (not shown) of another object with the substrate of the liquid crystal display panel 14, and outputs the signal potential given to two or more signal lines in 1 division block by time series. Corresponding to this, k time division switches 30-1 - 30-k are prepared in the input stage of the signal line 12-1 for n train - 12-n.

[0019] In order to realize 3 time sharing, a time division switch 30-1 consists of three CMOS analog switches (transmission switch) 31, 32, and 33 with which it connects with juxtaposition and a PchMOS transistor and a NchMOS transistor become, and is formed of the thin film transistor on the same substrate as the liquid crystal display panel 14 so that especially clearly from drawing 2 . Also about other time division switches 30-2 - 30-k, it has the completely same composition as a time division switch 30-1.

[0020] And, for example in the time division switch 30-1, each input edge of three analog switches 31, 32, and 33 is connected in common, and the common node is connected to the outgoing end of TABIC 28-1 through the common signal line 34-1. Thereby, it is TABIC (1). The signal potential outputted by time series is given to each input edge of three analog switches 31, 32, and 33 via the common signal line 34-1 from 28-1. Each outgoing end of these analog switches 31, 32, and 33 is connected to one edge each of three signal lines 12-1, 12-2, and 12-3.

[0021] To a time division switch 30-2, it goes via the common signal line 34-2, and is TABIC (2). The signal potential of time series is supplied from 28-2. Similarly, to time division switch 30-k, it goes via common signal-line 34-k, and is TABIC (k). The signal potential of time series is supplied from 28-k. In addition, although the configuration which allotted one common signal line per TABIC was shown by this example since it was easy, two or more common signal lines will be allotted actually.

[0022] Moreover, 2 per analog switch and a total of six control lines 35-1 to 35-6 are wired along the wiring direction of the gate line 11-1 - 11-m on the same substrate as the liquid crystal display panel 14. And if it is in a time division switch 30-1, for example, two control-input edges of an analog switch 32 are connected to a control line 35-3 and 35-4, and two control-input edges of an analog switch 33 are connected to a control line 35-1 and 35-2 for two control-input edges (namely, each gate of Nch and a PchMOS transistor) of an analog switch 31 a control line 35-5 and 35-6, respectively.

[0023] In addition, although the connection relation to six control lines 35-1 to 35-6 of three analog switches 31-33 of a time division switch 30-1 was explained, it has connection relation with the same completely said of other time division switches 30-2 - the 30-k here.

[0024] The selection pulses S1-S3 for choosing three analog switches 31-33 each of a time division switch 30-1 - 30-k, and XS1-XS3 are given from the outside to six control lines 35-1 to 35-6. Here, the selection pulses XS1-XS3 are reversal pulses of the selection pulses S1-S3. These selection pulses S1-S3, and XS1-XS3 are the signals for carrying out sequential ON of the three analog switches 31-33 each of a time division switch 30-1 - 30-k synchronizing with the signal potential of the time series outputted from each of TABIC 28-1 - 28-k.

[0025] In the liquid crystal display concerning the 1st operation gestalt of the above-mentioned configuration, the vertical-drive circuit 18 has a shift register, a level shifter, and a buffer, and vertical reversal of the scanning direction (driving direction) is attained the composition which can be scanned bidirectionally. The scanning direction is decided by the shift direction (direction of transfer) of a shift register.

[0026] An example of the circuitry of the shift register used for this vertical-drive circuit 18 is shown in drawing 3 . Each transfer stage serves as circuitry which consists of a latching clocked inverter, and the shift register concerning this example indicates the circuitry of transfer [the n+1st step of] stage to be the n-th step to drawing 3 . Here, the circuitry of transfer [the n-th step of] stage shall be taken and explained to an example.

[0027] In drawing 3 between the VDD line 41 and the GND line 42 The PMOS transistors Qp11 and Qp12 and the NMOS transistors Qn11 and Qn12 are connected to a serial. And each gate of the PMOS transistor Qp11 and the NMOS transistor Qn12 is connected in common. The clocked inverter 43 is constituted by impressing Clock CK to the gate of the PMOS transistor Qp12, and impressing Clock XCK (opposite phase of Clock CK) to the gate of the NMOS transistor Qn11, respectively.

[0028] Similarly, between the VDD line 41 and the GND line 42, the PMOS transistors Qp13 and Qp14 and the NMOS transistors Qn13 and Qn14 are connected to a serial, and each gate of the PMOS transistor Qp13 and the NMOS transistor Qn14 is connected in common, and the clocked inverter 44 is constituted by impressing Clock XCK to the gate of the PMOS transistor Qp14, and impressing Clock CK to the gate of the NMOS transistor Qn13, respectively.

[0029] In the configuration mentioned above, a transfer pulse is given to the common gate node of the PMOS transistor Qp11 which is the input edge of a clocked inverter 43, and the NMOS transistor Qn12 through the transfer line 45 from the transfer stage of the preceding paragraph (n-1 step). And the drain common node of the PMOS transistor Qp14

which is the outgoing end of a clocked inverter 44, and the NMOS transistor Qn13 is connected at the drain common node of the PMOS transistor Qp12 which is the outgoing end, and the NMOS transistor Qn11.
[0030] Moreover, CMOS inverter 46 which consists of the PMOS transistor Qp15 and the NMOS transistor Qn15 to which it connected with the serial and the gate was connected in common is formed between the VDD line 41 and the GND line 42. Parallel connection of this CMOS inverter 46 is carried out to hard flow to a clocked inverter 44, and it constitutes the latch circuit.
[0031] That is, the drain common node of the PMOS transistor Qp15 which is the outgoing end, and the NMOS transistor Qn15 is connected to the drain common node of the PMOS transistor Qp14 whose common gate node of the PMOS transistor Qp15 which is the input edge of CMOS inverter 46, and the NMOS transistor Qn15 is the outgoing end of a clocked inverter 44, and the NMOS transistor Qn13 at the common gate node of the PMOS transistor Qp14 which is the input edge of a clocked inverter 44, and the NMOS transistor Qn13, respectively.
[0032] The latch output of a latch circuit which consists of a clocked inverter 44 and CMOS inverter 46 is outputted to the transfer line 48 through CMOS inverter 47 which consists of the PMOS transistor Qp16 and the NMOS transistor Qn16 by which connected with the serial and the gate was connected in common between the VDD line 41 and the GND line 42.
[0033] ...., n-2 steps, n steps, n+2 steps, each input edge of .., and each outgoing end of .., n-1 step, n+1 step, and .. are connected to the transfer line 45, respectively. Moreover, each outgoing end of ...., n-2 steps, n steps, n+2 steps, and .., and .., n-1 step, n+1 step and each input edge of .. are connected to the transfer line 48, respectively.
[0034] CMOS switch 49n is allotted between the input edge of the transfer line 45, for example, transfer [the n-th step of] stage, and the outgoing end of transfer [the n+1st step of] stage, and CMOS switch 50n is allotted between the transfer line 48, for example, n steps of outgoing ends, and n+1 step of input edge. And the control signal (DC bias) for controlling a direction of transfer is given to the CMOS switches 49n and 50n through control lines 51 and 52.
[0035] Next, the circuit actuation for every direction of transfer of the vertical-drive circuit 18 which can be scanned in both directions of the above-mentioned configuration is explained.
[0036] First, the case of the transfer to down [down / of drawing 1], i.e., the left from the right of drawing 4 R> 4, is explained using drawing 4 . In the transfer to down [this], the DC bias of "H" level and a control line 52 serves as [the DC bias of a control line 51] "L" level. Then, in transfer [the n-th step of] stage, an OFF state and CMOS switch 50n will be [CMOS switch 49n] in an ON state. Moreover, in transfer [the n+1st step of] stage, CMOS switch 49n+1 will be in an ON state, and CMOS switch 50n+1 will be in an OFF state.
[0037] In this condition, the transfer pulse outputted from transfer [the n-1st step of] stage After being inputted into transfer [the n-th step of] stage and passing through this transfer [the n-th step of] stage, it is inputted into transfer [the n+1st step of] stage via CMOS switch 50n. CMOS switch 49n+1 after passing through this transfer [the n+1st step of] stage -- going -- transfer [the n+2nd step of] stage -- ** -- it will be transmitted leftward (the direction of an arrow head in drawing) in order from the right of drawing at the condition to say.
[0038] Next, the case of the transfer to above [above / of drawing 1], i.e., the right from the left of drawing 5 R> 5, is explained using drawing 5 . Besides, in the transfer to a direction, the DC bias of "L" level and a control line 52 serves as [the DC bias of a control line 51] "H" level. Then, in transfer [the n+1st step of] stage, CMOS switch 49n+1 will be in an OFF state, and CMOS switch 50n+1 will be in an ON state. Moreover, in transfer [the n-th step of] stage, an ON state and CMOS switch 50n will be [CMOS switch 49n] in an OFF state.
[0039] In this condition, the transfer pulse outputted from transfer [the n+2nd step of] stage It is inputted into transfer [the n+1st step of] stage via CMOS switch 50n+1. After passing through this transfer [the n+1st step of] stage, it is inputted into transfer [the n-th step of] stage via CMOS switch 49n. CMOS switch 50n-1 after passing through this transfer [the n-th step of] stage -- going -- transfer [the n-1st step of] stage -- ** -- it will be transmitted rightward (the direction of an arrow head in drawing) in order from the left of drawing at the condition to say.
[0040] In the vertical-drive circuit of the above-mentioned configuration, as a control signal which controls a scanning direction, a DC bias will only be given to control lines 51 and 52, and a scanning direction can be controlled easily.
[0041] Thus, by using the vertical-drive circuit which can be scanned bidirectionally as a vertical-drive circuit 18 of drawing 1 TABIC (1) which is an external IC circuit 28-1 - TABIC(k)28-k -- a user -- liking -- responding -- the upper and lower sides of the liquid crystal display panel 14, even if it arranges to any In order for what is necessary just to be to change the scanning direction of the vertical-drive circuit 18 according to the arrangement even if it does not prepare the field memory for performing an image data list substitute outside, it is low cost and a flexible liquid crystal module becomes possible.
[0042] In addition, as shown in drawing 1 , although [this operation gestalt] the vertical-drive circuit 18 in which a bidirectional scan is possible is arranged only to one side (left-hand side) to the pixel section of the liquid crystal display panel 14, you may make it arrange the vertical-drive circuits 18A and 18B of the couple in which both bidirectional scans are possible on both sides of the pixel section of the liquid crystal display panel 14, as shown in

drawing 6 .
[0043] Thus, since a scan pulse can be inputted from the both sides of the liquid crystal display panel 14 when the vertical-drive circuits 18A and 18B in which a bidirectional scan is possible have been arranged on both sides of the pixel section of the liquid crystal display panel 14, the difference according to the pixel location in the horizontal direction of the propagation delay of the scan pulse resulting from wiring resistance etc. can be made small. Moreover, the configuration of the liquid crystal display panel 14 can be made into bilateral symmetry.
[0044] Moreover, in this operation gestalt, although one vertical-drive circuit 18 (18A, 18B) considered as the configuration in which a bidirectional scan is possible, as shown in drawing 7 , it is able for a scanning direction to arrange the vertical-drive circuits 18a and 18b of the couple of a uni-directional scan of an opposite direction on both sides of the pixel section of the liquid crystal display panel 14, to double both, respectively, and to consider as the vertical-drive circuit in which a bidirectional scan is possible.
[0045] Also in this case, since the circuit of the same configuration will be arranged at the both sides of the liquid crystal display panel 14, the configuration of the liquid crystal display panel 14 can be made into bilateral symmetry. In addition, what is necessary is to constitute the selection so that supply voltage may be selectively supplied with a switch etc., and just to make it forbid supply of supply voltage in the vertical-drive circuit of those who do not use it with the switch concerned, although it is the translation which uses only either of the vertical-drive circuits 18a and 18b of a couple.
[0046] In addition, although considered as the configuration using the time-sharing actuation by the time division switch 30-1 - 30-k in the liquid crystal display concerning this operation gestalt, it is possible to apply also like the liquid crystal display of a configuration of that it is not limited to this configuration and each output of TABIC 28-1 - 28-k, and the signal line 12-1 of the liquid crystal display panel 14 - 12-n have the response relation of 1 to 1.
[0047] Drawing 8 is the outline block diagram showing the liquid crystal display concerning the 2nd operation gestalt of this invention, among drawing, gives the same sign to drawing 1 and an equivalent part, and is shown. In this operation gestalt, it has composition which builds in the level shifter 36 which is a booster circuit in the liquid crystal display panel 14, carries out pressure up to the electrical potential difference of the high level which exceeds 5V, for example for the electrical potential difference of the low not more than 5V given from the outside, and supplies the vertical-drive circuit 18.
[0048] By the way, in the component used for a liquid crystal display like a-Si (amorphous silicon) or poly-Si (polish recon), generally, since it is high compared with LSI usual in the threshold voltage Vth, the actuation level as an external interface becomes high. On the other hand, the power source of the surrounding drive system of the liquid crystal display panel 14 is in the inclination of low-battery-izing for the purpose of reduction of power consumption.
[0049] However, positive actuation of the vertical-drive circuit 18 can be realized, maintaining low-battery-ization of the circumference drive system of the liquid crystal display panel 14 by having built in the level shifter 36 in the liquid crystal display panel 14, carrying out pressure up of the electrical potential difference given from the outside, and having made it supply the vertical-drive circuit 18 like the liquid crystal display concerning this operation gestalt.
[0050] An example of the circuitry of the level shifter of a differential mold is shown in drawing 9 . In drawing 9 , the constant current source is constituted between the VDD line 61 and the GND line 62 by connecting the PMOS transistor Qp21 and the NMOS transistor Qn21 to the serial, connecting the gate and the drain of the PMOS transistor Qp21 in common, and connecting the gate of the NMOS transistor Qn21 to the VDD line 61.
[0051] The electrical potential difference from the outside is inputted between an input terminal 63 and 64, an input terminal 63 is a high-level side, and an input terminal 64 is on a low side. Between the VDD line 61 and an input terminal 63, the PMOS transistor Qp22 and the NMOS transistor Qn22 are connected to a serial, and the PMOS transistor Qp23 and the NMOS transistor Qn23 are further connected to the serial. Each gate of the PMOS transistors Qp22 and Qp23 is connected as in common as the gate (drain) of the PMOS transistor Qp21.
[0052] Moreover, between the VDD line 61 and an input terminal 64, the PMOS transistor Qp24 and the NMOS transistor Qn24 are connected to a serial, and the PMOS transistor Qp25 and the NMOS transistor Qn25 are further connected to the serial. And the gate and the drain of the PMOS transistor Qp24 are connected with the gate of the PMOS transistor Qp23 in common, and the gate of the NMOS transistor Qn24 is connected with the gate of the NMOS transistor Qn22, and a drain in common. Moreover, the gate and the drain of the NMOS transistor Qn25 are connected with the gate of the NMOS transistor Qn23 in common.
[0053] In the differential mold level shifter of the above-mentioned configuration, supposing the electrical potential difference of the VDD line 61 is 12V, the level shift of the electrical potential difference an input terminal 63 and whose amplitude inputted among 64 are 3V will be carried out to the electrical potential difference whose amplitude is 12V, and it will be outputted to the vertical-drive circuit 18 from an output terminal 65. In addition, it does not pass over the circuitry mentioned above to an example, but it can use the thing of various circuitry as a level shifter 36.
[0054]

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the outline block diagram showing the liquid crystal display concerning the 1st operation gestalt of this invention.
[Drawing 2] It is the enlarged drawing of the important section of drawing 1 .
[Drawing 3] It is the circuit diagram showing an example of the configuration of the shift register of the vertical-drive circuit in which a bidirectional transfer is possible.
[Drawing 4] It is a circuit diagram for explaining the circuit actuation in a down transfer.
[Drawing 5] It is a circuit diagram for explaining the circuit actuation in an above transfer.
[Drawing 6] It is the outline block diagram showing the modification of the 1st operation gestalt.
[Drawing 7] It is the outline block diagram showing other modifications of the 1st operation gestalt.
[Drawing 8] It is the outline block diagram showing the liquid crystal display concerning the 2nd operation gestalt of this invention.
[Drawing 9] It is the circuit diagram showing an example of the configuration of the level shifter of a differential mold.
[Drawing 10] It is the outline block diagram of the system which has a field memory outside.
[Description of Notations]
11-1 - 11-m [-- A liquid crystal display panel, 18, 18A, 18B / -- The vertical-drive circuit of a bidirectional scan, 18a, 18b / -- The vertical-drive circuit of a uni-directional scan, 22 / -- A level actuation circuit, 30-1 - 30-k / -- A time division switch, 31-33 / -- Analog switch] -- A gate line, 12-1 - 12-n -- A signal line, 13 -- A pixel, 14

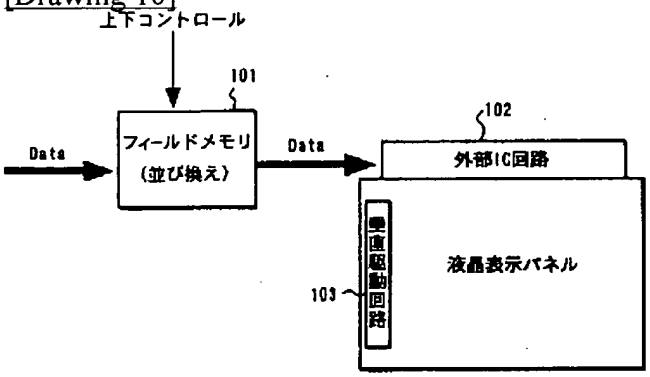
[Translation done.]

* NOTICES *

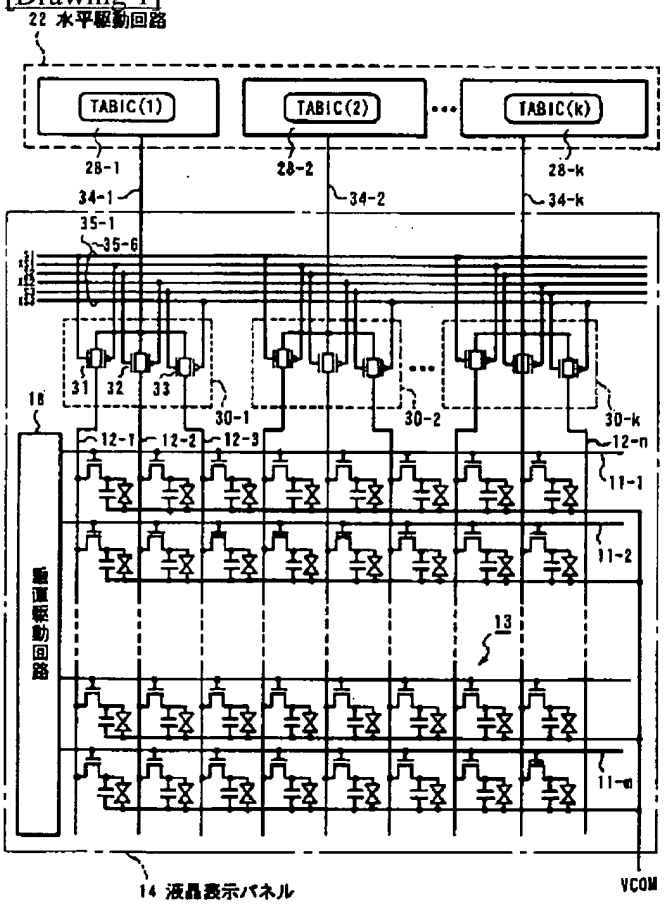
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

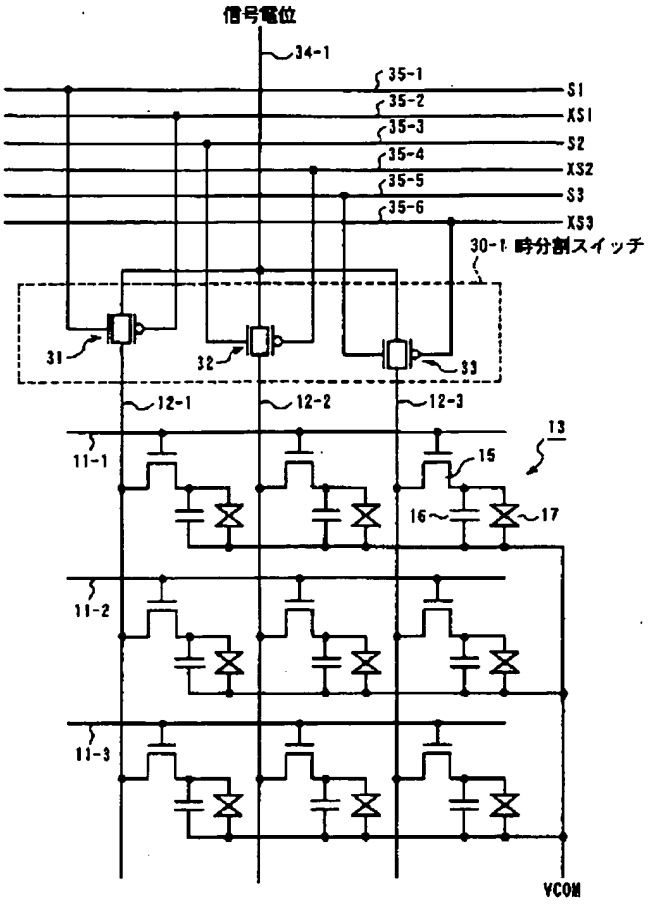
[Drawing 10]



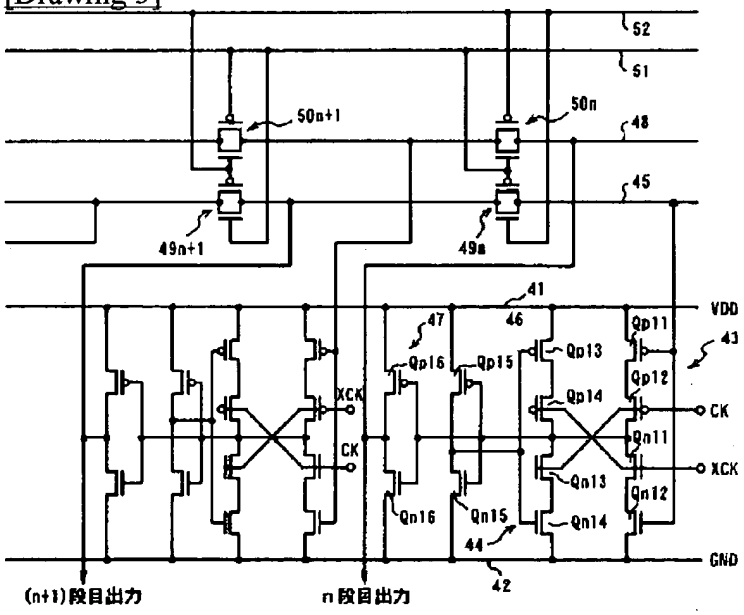
[Drawing 1]



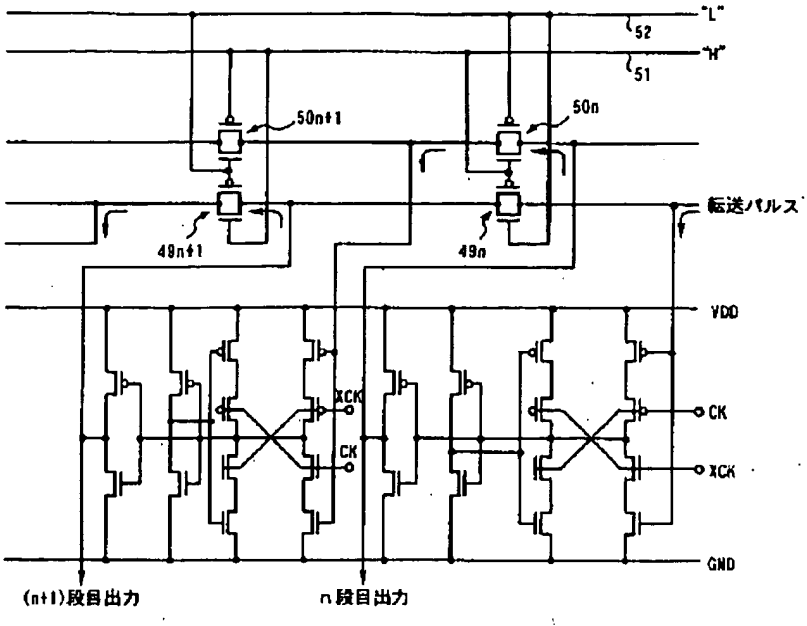
[Drawing 2]



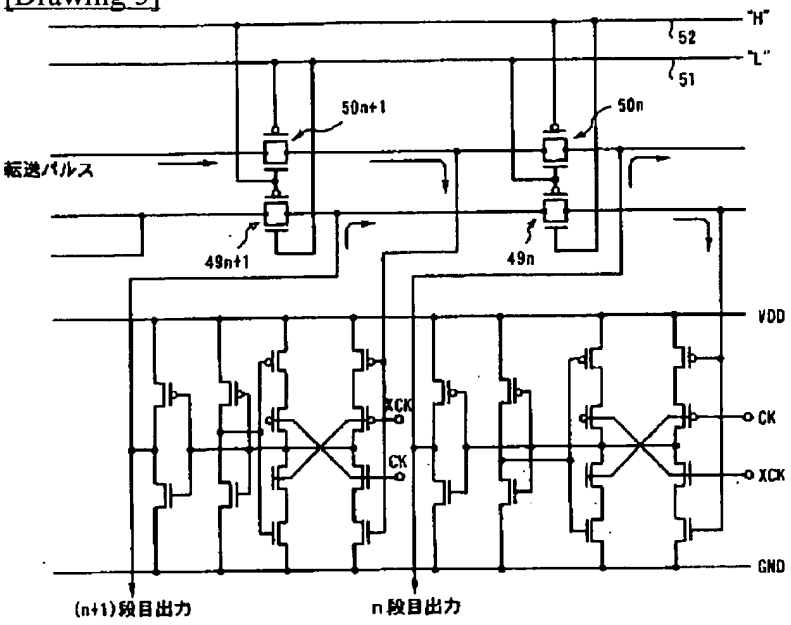
[Drawing 3]



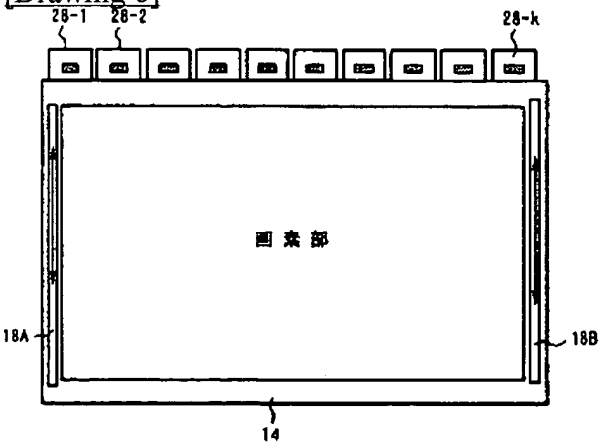
[Drawing 4]



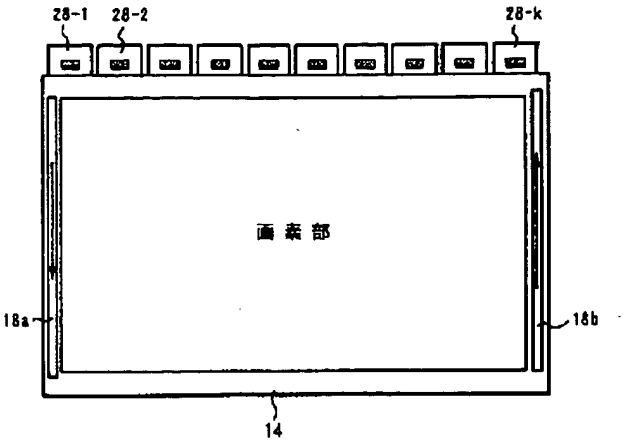
[Drawing 5]



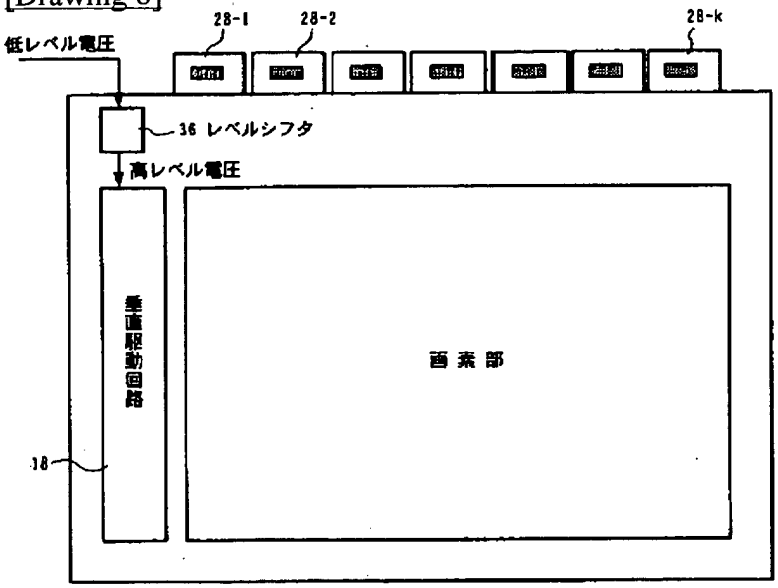
[Drawing 6]



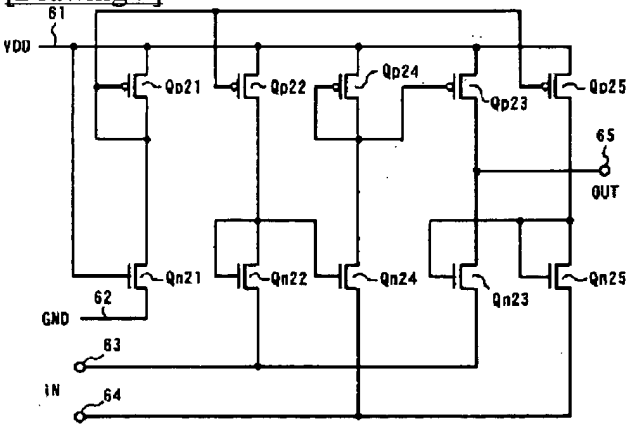
[Drawing 7]



[Drawing 8]



[Drawing 9]



[Translation done.]